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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/665,468	09/22/2003	Ikuo Yasui	67161-104	5516

7590 10/30/2006

McDermott, Will & Emery
600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER	
EJAZ, NAHEED	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/30/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/665,468	YASUI ET AL.	
	Examiner	Art Unit	
	Naheed Ejaz	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claim 1 is rejected under 35 U.S.C. 102(e) as being anticipated by Filipovic (2005/0078596).

3. Regarding claim 1, Filipovic discloses, 'variable gain amplifier circuit (figure 5, element 46) amplifying said signal received at an antenna to change a level of said signal to a prescribed level' (figure 2, element 20, figure 3, element 22); a gain control circuit outputting a gain control amount to said variable gain amplifier circuit (figure 5, element 49) to control a gain of said signal in said variable gain amplifier circuit (paragraph # 0054-0055); and a register storing an initial value of said gain control amount set from outside (figure 5, element 62), wherein said gain control circuit starts to control said gain at each reception frame, using said initial value stored in said register' (paragraphs # 0054-0056).

4. Refer to claim 2, Filipovic teaches that is resetting the accumulator 60 (figure 5) value if new packets are received by wireless communication device (WCD 10) (claimed

'reception apparatus is reset') which are inputted to the gain control register 62 (figure 5, paragraph # 0058) (claimed 'initial value is set to said register from said outside').

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3-5 & 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazecki et al. (4,930,126) in view of Yokozaki et al. (5,448,774) (hereinafter, Kazecki and Yokozaki respectively).

7. Refer to claim 1, Kazecki teaches, 'a variable gain amplifier circuit amplifying said signal received at an antenna to change a level of said signal to a prescribed level' (figure 2, element 78), 'a gain control circuit outputting a gain control amount to said variable gain amplifier circuit to control a gain of said signal in said variable gain amplifier circuit' (figure 2, element 80, col.3, lines 25-31), 'a register storing an initial value of said gain control amount set from outside' (figure 2, elements 66 & 76, col.3, lines 35-51), wherein said gain control circuit starts to control said gain at each reception frame' (col.3, lines 20-51).

Kazecki does not teach gain control according to the initial value stored in register.

Yokozaki teaches, 'gain control circuit starts to control said gain using said initial value stored in said register' (figure 1, elements 14 & 15, figure 3, col.4, lines 9-19) (it is

noted in the mentioned column figure 3(f) shows the gain control according to the contents of the memory 21 (figure 2) which reads on claim limitations since memory (claimed 'register') is responsible to store the values (could be claimed 'initial value', col.4, lines 34-35) in order to control the gain (claimed 'control said gain using said initial valued').

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Yokozaki into Kazecki in order to control the gain according with the detected level without affecting the reception of desired signals as taught by Yokozaki (col.1, lines 57-68, col.2, lines 1-6) thus reduce disturbance of reception when a large input signal is received and enhance system performance.

8. Refer to claim 3, Kazecki teaches all the limitations in the previous claim on which claim 3 depends but he fails to disclose signal level detection circuit.

Yokozaki discloses, 'a signal level detect circuit detecting said level of said Signal' (figure 1, element 14); wherein said gain control circuit includes a holding circuit taking in said initial value from said register to hold' (figure 1, element 14), and said gain control circuit (figure 1, element 15) starts to control said gain using said initial value that is held in said holding circuit, and subsequently, determines said gain control amount in accordance with said level of said signal that is detected by said signal level detect circuit, and outputs the determined gain control amount to said variable gain amplifier circuit at each reception frame' (figure 1, elements 2 & 15, col.3, lines 20-41).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Yokozaki into Kazecki in order to control the

gain according with the detected level without affecting the reception of desired signals as taught by Yokozaki (col.1, lines 57-68, col.2, lines 1-6) thus reduce disturbance of reception when a large input signal is received and enhance system performance.

9. Refer to claim 4, in addition to aforementioned rejection of claim 3, Kazecki discloses that the end of data corresponding to information received during slot 12 (figure 1) is clocked from digital storage 76 (figure 2) just prior to the next slot 12 so that the gain and level associated with elements 70 and 72 (figure 2) are equal to the magnitude and gains associated with the end of the preceding slot 12 (col.3, lines 39-51) which is equivalent to the claim limitations of 'initial value from said register at an end of said reception frame, and holds the taken in initial value until next reception frame'.

10. With respect to claim 5, Kazecki teaches all the limitations in the previous claim on which claim 5 depends but he fails to disclose holding circuit holds the expiration of a prescribed period.

Yokozaki discloses, 'holding circuit further holds said gain control amount at an expiration of a prescribed period from a start of said reception frame' (figure 3, col.3, lines 27-50), said gain control circuit outputs, before the expiration of said prescribed period, said gain control amount that is determined in accordance with said level of said signal detected by said signal level detect circuit to said variable gain amplifier circuit' (figure 3, col.3, lines 51-68, col.4, lines 1-35), and said gain control circuit outputs, after the expiration of said prescribed period, said gain control amount at the expiration of said prescribed period that is held by said holding circuit to said variable gain amplifier

circuit' (figure 3, col.3, lines 51-68, col.4, lines 1-35) (it is noted that in the mentioned columns and lines that Yokozaki is detecting the signal with respect to the predetermined level by using the detecting and holding circuit 14 (figures 1 & 2) (col.3, lines 27-41) (claimed 'holds said gain control amount'). Furthermore, he is performing the reception when the signal is at high level which has time duration associated with (claimed 'prescribed period') and no reception when the level is low (claimed 'expiration of said prescribed period') (col.3, lines 51-65) with respect to control signal operation and therefore reads on claim limitations).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Yokozaki into Kazecki in order to control the gain according with the detected level without affecting the reception of desired signals as taught by Yokozaki (col.1, lines 57-68, col.2, lines 1-6) thus reduce disturbance of reception when a large input signal is received and enhance system performance.

11. Refer to claim 10, Kazecki teaches all the limitations in the previous claim on which claim 10 depends but he fails to disclose attenuation.

Yokozaki teaches, 'an attenuation amount of said signal propagating from a transmission apparatus transmitting said signal to said reception apparatus' (figure 5, element 16, col.5, lines 19-28).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Yokozaki into Kazecki in order to control the gain according with the detected level without affecting the reception of desired signals

as taught by Yokozaki (col.1, lines 57-68, col.2, lines 1-6) thus reduce disturbance of reception when a large input signal is received and enhance system performance.

12. Claims 6 & 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kazecki et al. (4,930,126) in view of Yokozaki et al. (5,448,774), as applied to claims 1, 3 & 5 above, and further in view of Kinoshita (5,768,698).

13. Refer to claim 6, Kazecki and Yokozaki teach all the limitations in the previous claim on which claim 6 depends but they fail to disclose period generator circuit.

Kinoshita teaches, 'a period generator circuit generating said prescribed period' (figure 3, element 73 & figure 6, element 72), wherein said period generator circuit notifies said gain control circuit of said prescribed period' (figure 3, elements 7 & 73, figure 6, elements 7 & 72) (col.13, lines 7-39).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Kinoshita into Kazecki and Yokozaki in order to control the variable gain in response to every entry of sampling data thus increasing an overall receiving performance of the receiving system as taught by Kinoshita (col.2, lines 30-40, col.4, lines 24-26).

14. Regarding claim 7, Kazecki and Yokozaki teach all the limitations in the previous claim on which claim 7 depends but they fail to disclose period generator circuit includes a timer.

Kinoshita teaches, 'period generator circuit includes a timer for measuring said prescribed period' (figure 2, element 72) (see claim 6 rejection above).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Kinoshita into Kazecki and Yokozaki in order to control the variable gain in response to every entry of sampling data thus increasing an overall receiving performance of the receiving system as taught by Kinoshita (col.2, lines 30-40, col.4, lines 24-26).

15. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazecki et al. (4,930,126) in view of Yokozaki et al. (5,448,774), as applied to claims 1, 3 & 5 above, and further in view of Glover (6,101,229).

16. Regarding claim 8, Kazecki teaches 'time division signal' and frame timing (figure 2, element 46, col.3, lines 32-42) but Kazecki and Yokozaki do not teach header information.

Glover discloses, 'header information, and said prescribed period is a period for receiving said header information' (figure 2, element 40, col.2, lines 64-67, col.7, lines 23-33).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Glover into Kazecki and Yokozaki in order to provide gain and timing recovery signal for channels thus achieve data synchronization in the circuit as taught by Glover (col.2, lines 64-67 & col.3, lines 23-35).

17. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kazecki et al. (4,930,126) in view of Yokozaki et al. (5,448,774), as applied to claims 1 & 3 above, and further in view of Tomita (4, 274,117).

18. Regarding claim 9, in addition to aforementioned rejection of claim 3, Kazecki & Yokozaki teach all the limitations in the previous claim on which claim 9 depends but they fail to disclose first and second signal level detecting circuits.

Tomita discloses, 'a first signal level detect circuit detecting a level of the signal (figure 3, element 4) that is amplified by said variable gain amplifier circuit; and a second signal level detect circuit detecting a level of the signal (figure 3, element 10) (col.4, lines 18-42, col.6, lines 54-65) before input to said variable gain amplifier circuit; wherein said gain control circuit compares first and second signal levels detected by said first and second signal level detect circuits, respectively, (figure 3, element 15) determines said gain control amount based on a result of the comparison, and outputs said determined gain control amount to said variable gain amplifier circuit' (figure 3, element 3, col.4, lines 49-61).

It would have been obvious to one of ordinary skill in the art, at the time of invention, to implement the teachings of Tomita into Kazecki and Yokozaki in order to provide the reference information for performing level setting with respect to input level at which the gain circuit would start attenuation as taught by Tomita (col.4, lines 29-33) thus provide stable gain for the circuit.

Contact Information

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naheed Ejaz whose telephone number is 571-272-5947. The examiner can normally be reached on Monday - Friday 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on 571-272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Naheed Ejaz
Examiner
Art Unit 2611

N.E.
10/25/2006

PANKAJ KUMAR
PRIMARY PATENT EXAMINER